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Efficient Afir Filter Based On Distributed Arithmetic

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Abstract: The Finite Impulse Response digital filter is widely used as a basic tool in various signal time realization of FIR (Finite Impulse Response filter) with less hardware requirement and less latency has become more and more important. The design method of MAC (multiplication and accumulation) operation is the core of FIR filter implementation. Distributed Arithmetic is an important technique to implement digital signal processing (DSP) functions in FPGA (Field Programmable Gate Arrays). It provides an approach for multiplier-less implementation of FIR filter, since it is an algorithm that can perform multiplication with use of LUT (look Up Table) that stores the pre-computed values and can be read out easily which makes DA (Distributed Arithmetic)based computation well suited for FPGA realization, because the LUT is the basic component of FPGA. The major disadvantage of DA technique is that the size of Da-LUT increased exponentially with the increasing length of input. Several efforts have been made to reduce the Da-LUT size for efficient realization of DA-based designs. In this paper, LUT is partitioned into smaller size LUT, so that the LUT size can be reduce to one fourth (the size of the table is reduced from one 4N*2B LUT to four N*2B tables). Hence the length of the LUT can be reduced.

Keywords: Distributed Arithmetic, Finite Impulse Response, Look Up Table.

I. INTRODUCTION

A digital filter is a system that performs mathematical operations on a sampled or discrete time signal to reduce or enhance certain aspects of that signal. One type of digital filter is FIR filter. It is a stable filter. It gives linear phase response Pipelining and parallel processing technique is used in FIR filter. Pipelining operation takes place in an interleaved manner. Pipelining done by inserting latches (delay element) in the system, it increased the overall speed of the architecture but the hardware structure and system latency will increase. Hardware structures increased due to inserting pipelining latches. For M-level pipelining M-1 delay elements required. Latency is the difference between the availability of first output in the sequential system and pipeline system. At every clock cycle it will operate multiple inputs and produced multiple outputs is called parallel processing. It required extra hardware. Both pipelining and parallel processing has disadvantages. For IFR filters, output is a linear convolution of weights and inputs. For an Nth order FIR filter, the generations of each output sample takes N+1 multiply accumulate (MAC) operations. Multiplication is strongest operation because it is repeated addition. It require large portion of chip area. Power consumption is more. Memory based structures are more regular compared with the multiply accumulate structures, and have many other advantages, e.g., greater potential for high throughput and reduced---latency implementation and are expected to have less dynamic power consumption due to less switching activities for memory read operations compared to the conventional multipliers. Memory based structures are well suited for many digital signal processing (DSP) algorithms, which involve multiplication with a fixed set of coefficients. For this distributed. Arithmetic is one way to implement convolution with multiplier less unit, where the MAC operations are replaced by a series of LUT access and summations. Distributed Arithmetic is a different approach for implanting digital filters. The basic idea is to replace all multiplications and additions by a table and a shifter accumulator. LUT are the kind of logic that used in SRAM based FPGAs. Basically each look table is a bunch of single bit memory cells storing individual bit values in each of the cells. Memory access time is less in SRAM, so speed of the static RAM is high. Distributed Arithmetic provides cost effective and area time efficient computing structures. Digital finite Impulse Response (FIR) filters are essential building blocks in most Digital Signal Processing (DSP) systems. A large application is telecommunication where filters are needed in receivers and transmitters, and an increasing portion of the signal processing is done digitally. However, power dissipation of the digital parts can be a limiting factor, especially in portable, battery operated devices. Scaling of the feature sizes and supply voltages naturally helps us to reduce power. For a certain technology, there are still many kinds of architectural and implementation approaches available to the designer. Due to the advancement in Very Large Scale Integration (VLSI) technology, realization of FIR filters is done in Application Specific Integrated Circuits (AIC) and Field Programmable Gate Arrays (FPGA) platforms.

II. LUT DESIGN FOR MEMORY BASED MULTIPLLICATION

The basic principle of memory-based multiplication is depicted in Fig1. Let A be a fixed coefficient and X be an input word to be multiplied with A. If we assume X to be an unsigned binary number of word-length L, there can be

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possible values of X, and accordingly, there can be possible values of product C=A.X.

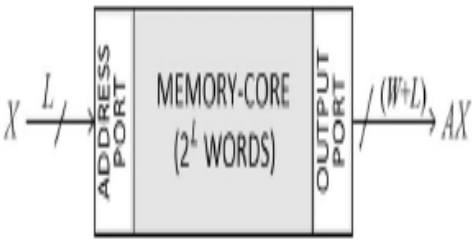

Figure1. LUT based multiplier

Therefore, for the conventional implantation of memory-based multiplication, a memory unit of words is required to e used as look-up table consisting of pre-computed product values corresponding to all possible values of X. The product-word A, for 0 -1, is stored at the memory location whose address I s the same as the binary value, such that if L-bit binary value of is used as address for the memory-unit, then the corresponding Product value is read-out from the memory.

III. DISTRIBUTED ARITHMETIC

In Distributed Arithmetic concept the LUT size is increasing exponentially, the LUT size will be 2^n. The LUT is partitioned into smaller size LUT, so that the LUT size can be reduced to one fourth (The size of the table is reduced from one 4N*2B LUT to four N*2B tables). Hence the length of the LUT can be reduced.

Here pipeline architecture is used to increase the speed of the design. Pipeline process in nothing but, it fetches the next data while the current computation is executing, the basic DA architecture which is implemented in three main stages i.e. shift register units, LUT unit, and the shift and add unit. This architecture represents a 16-tap FIR filter. In this case, the LUT size is (2^n=256) where n is the filter order. Bute we are dividing LUT size form one 4N*2B to four N*2B so now the LUT size is 16, but we are using 4 LUTs.

IV. LUT LESS ARCHITECTURE

DA technique proves to be a powerful technique for implementing MAC unit as a multiplier less algorithm through the use of memory Rom or LUT to store a DA technique proves to be a powerful technique for

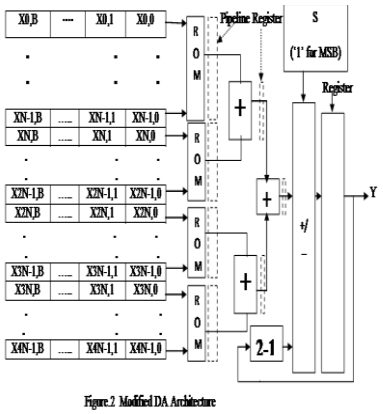

Figure.2 Modified DA Architecture

implementing MAC unit as a multiplier less algorithm through the use of memory ROM or LUT to store a pre-computed partial sum of inner products. Therefore, this computational efficiency made the DA popular various DSP applications in which one of the multiplication operands is fixed. Unfortunately, DA technique suffers from a major drawback i.e. the dramatic growth of LUT size when filter order of the number of input variables increase. This paper presents new structures for the distributed arithmetic LUT that provides the DA technique with the optimum solution for its major drawback. It made the LUT size independent of the filter order or the number of input variables.

The proposed structure of Da-based adaptive filter of length N=4 is shown in figure 6.1.

It consists of a four-point inner product and a weight increment block along with additional circuits for the computation of error value e(n) and control word t for the barrel shifters.

The four point inner product block includes a DA table consisting of an array of 15 registers which stores the partial inner products y 1 for 0<1<=15 and a 16:1 multiplexer (MUX) to select the content of one of those registers. Bit slices of weights A={w31 w21 w11 w01} are fed to the MUX as control in LSB-to-MSB order, and the output of the MUX is fed to the carry-save accumulator. After L bit cycles, the carry-save accumulator shift accumulates all the partial inner products and generates a sum word and a carry word of size (L+2) bit each. The carry and sum words are shifted added with an input carry "1" to generate filter output which is subsequently subtracted from the desired output d(n) to obtain the error e(n).

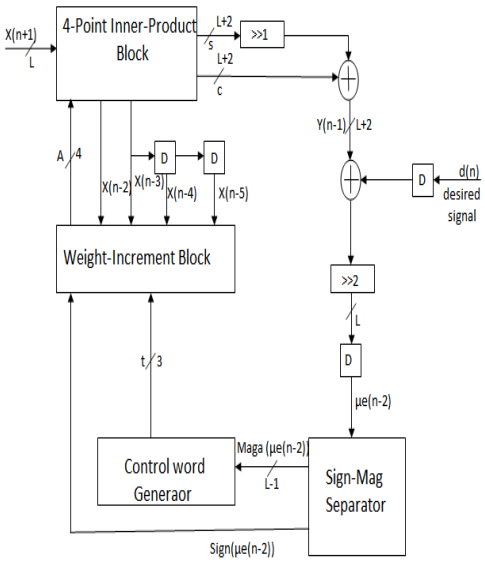

Figure3. Adaptive FIR filter

As in the case all the bits of the error except the most significant one are ignore, such that multiplication of input x k by the error is implemented by a right shift through the number of locations given by the number of leading zeros in the magnitude of the error. The magnitude of the computed error is decoded to generated the control word t for the barrel shifter.

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The logic used for the generation of control word t to be used for the barrel shifter. The convergence factorμ is usually taken to be O(1/N). We have taken μ=1/N. however, one can take μ as 2-i/N, where I is a small integer. The number of shifts t in that case is increased by I, and the input to the barrel shifter is pre-shifted by I locations accordingly to reduce the hardware complexity. The weight-increment unit consists of four barrel shifters and four adder or subtractor cells.

V. RESULT

The conventional DA based structure is designed and simulated in Modelsim which consumes more area whereas the proposed DA based structure is used as a combinational block. The 8bit LUT is designed and it occupies more area. Combinational block LUT is designed and it occupies low area, so this LUT is used in the proposed DA system. Simulation results of various LUT are shown in figure

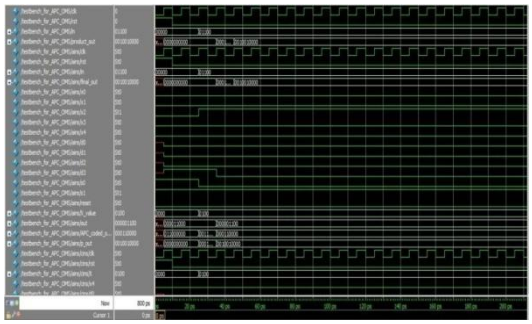

Fig Simulation results of AFIR filter

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